Low Cost, Single & Multi-Channel, Voltage-to-Frequency Converters

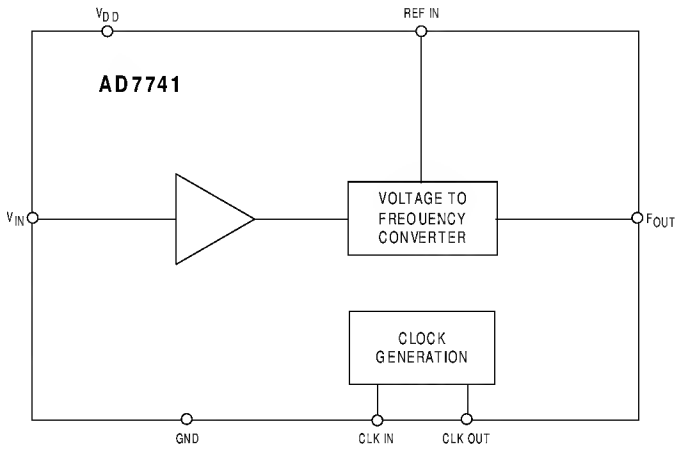
Preliminary Technical Data

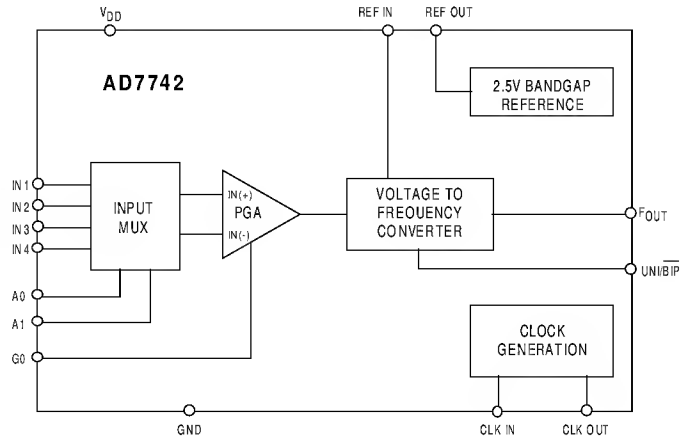
AD7741/42

FEATURES

Synchronous Operation
Full-Scale Frequency Set by External System Clock
Single +5V Supply Operation
AD7741: Single-ended input
AD7742: 2 Pseudo-Differential inputs + 1 Differential, OR 2 Fully Differential inputs
Input Signal Range selectable via Gain pin
No user intervention required to achieve specified performance
Input Signal Range:
AD7741: 0V to +REF IN
AD7742: Unipolar: 0V to +REF IN or
0V to +REF IN/2
Bipolar: -REF IN to +REF IN or
-REF IN/2 to +REF IN/2
Minimum External Components required
Low Power: 30 mW typ
AD7741: 8-Pin DIP, 8-Lead 0.15" wide SOIC packages
AD7742: 16-Pin DIP, 16-Lead 0.15" wide SOIC packages

FUNCTIONAL BLOCK DIAGRAMS





GENERAL DESCRIPTION

The AD7741 and AD7742 are a new generation of synchronous Voltage-to-Frequency Converters (VFC's). The AD7741 is a single-ended version in a small 8-pin DIP/SOIC package and the AD7742 is a multi-channel version in a 16-pin DIP/SOIC package. Small package, low cost, ease of use plus no user trims required to achieve specified performance were major design goals for these products.

The AD7742 contains an internal +2.5 V bandgap reference and offers two differential inputs or one differential and two pseudo-differential inputs. The AD7742 also allows the user the choice of pin-programming the channel and gain settings.

The AD7741 accepts a single-ended analog input range from 0 V to +REF IN and the AD7742 accepts differential analog input ranges from -REF IN to +REF IN. Both parts operate from a single +5 V supply consuming only 30 mW typical.

PRODUCT HIGHLIGHTS

1. The AD7741 is a single channel, single-ended VFC. It is available in an 8-pin DIP and in an 0.15" wide 8-lead SOIC package.
2. The AD7742 is a multi-channel VFC whose internal settings (PGA & Channel Select) can be pin selected by tying certain package pins high or low. It is available in an 16-pin DIP and in an 0.15" wide 16-lead SOIC package.
3. Low Power, Single Supply Operation
   The AD7741 and AD7742 operate from a single +5 V supply and consume only 30 mW.

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AD7741—PRELIMINARY SPECIFICATIONS

(V_{DD} = +5 V± 5%, GND = 0 V, External Reference = +2.5 V; XCLK IN = 5MHz; All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[2]	B Versions[1]	Y Versions[1]	Units	Test Conditions/Comments
ACCURACY				
Linearity Error				
$XCLK_{IN}$ = 200 kHz	±0.012	±0.012	% of Span max.	
$XCLK_{IN}$ = 2 MHz	±0.012	±0.012	% of Span max.	
$XCLK_{IN}$ = 5 MHz	±0.012	±0.012	% of Span max.	
DC ACCURACY				
DC Input Current	±1.0	±1.0	nA typ	100nA max.
DC Power Supply Rejection Ratio	0.001	0.001	%/V max	
Offset Error			µV max.	
Offset Error Drift			µV /°C typ.	
Gain Error	±0.5	±0.5	% of Span max.	
Gain Error Drift			ppm/°C typ.	
ANALOG INPUT				
Input Resistance			kΩ min	
Input Voltage Range	0V to +REF IN	0V to +REF IN	Volts	
VOLTAGE REFERENCE				
REF IN				
Input Voltage	2.5	2.5	V nom	
Input Resistance			kΩtyp	
LOGIC OUTPUT (F_{OUT})				
Output High Voltage, V_{INH}	2.4	2.4	V min	I Source = 800 µA except for $XCLK_{OUT}$
Output Low Voltage, V_{INL}	0.4	0.4	V max	I Sink = 1.6 mA except for $XCLK_{OUT}$
LOGIC INPUTS[3]				
ALL INPUTS EXCEPT $XCLK_{IN}$				
Input High Voltage, V_{INH}	2.0	2.0	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}	10	10	pF typ	
$XCLK_{IN}$ ONLY				
Input High Voltage, V_{INH}	3.5	3.5	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}	10	10	pF typ	
CLOCK FREQUENCY				
$XCLK_{IN}$	100	100	kHz min	For Specified performance
	5	5	MHz max	
POWER REQUIREMENTS				
V_{DD}	+5	+5	V nom	±5% for Specified Performance
I_{DD}	8	8	mA max	V_{DD} = 5V± 5%
Power Dissipation	40	40	mW max	Typically 30mW

NOTES
[1]Temperature Ranges are as follows: B Version, –40°C to +85°C; Y Version, –40°C to +125°C.
[2]See Terminology.
[3]Guaranteed by design and characterization, not production tested
Span = Max output frequency - Min output frequency
Specifications subject to change without notice.

AD7742-PRELIMINARY SPECIFICATIONS

(V_{DD} = +5 V ± 5%, GND = 0 V, External Reference = +2.5 V; XCLK IN = 5MHz; All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[2]	B Versions[1]	Y Versions[1]	Units	Test Conditions/Comments
ACCURACY				
Linearity Error				
$XCLK_{IN}$ = 200 kHz	±0.012	±0.012	% of Span max.	
$XCLK_{IN}$ = 2 MHz	±0.012	±0.012	% of Span max.	
$XCLK_{IN}$ = 5 MHz	±0.012	±0.012	% of Span max.	
Channel-to-Channel Isolation			dB typ	V_{IN} ?=kHz
DC ACCURACY				
DC Input Current	±1.0	±1.0	nA typ	100nA max.
DC Power Supply Rejection Ratio	0.001	0.001	%/V max	
Unipolar Offset Error			µV max.	
Unipolar Offset Error Drift			µV/°C typ.	
Unipolar Gain Error	±0.5	±0.5	% of Span max.	
Unipolar Gain Error Drift			ppm/°C typ.	
Bipolar Offset Error	±100	±100	µV max.	
Bipolar Zero Error			µV max.	
Bipolar Gain Error	±0.5	±0.5	% of Span max.	
CMR			dB	
ANALOG INPUT				
Input Resistance			kΩmin	
Common Mode Range[4]	-300mV to V_{DD} - 2V	-300mV to V_{DD} - 2V	Volts	
Differential Input Voltage Range	±REF/Gain	±REF/Gain	Volts	Bipolar Input Range
	0 to REF/Gain	0 to REF/Gain	Volts	Unipolar Input Range
VOLTAGE REFERENCE				
REF IN				
Input Voltage	2.5	2.5	V nom	
Input Resistance			kΩ typ	
REF OUT				
Output Voltage	2.4/2.6	2.4/2.6	V min/V max	2.5 V ± 5%
Drift	100	100	ppm/°C typ	
Line Regulation			µV/V max	
Load Regulation			µV/mA max	
Noise (0.1 Hz - 10 Hz)			µV (p-p) typ	
Output Resistance	100	100	kΩtyp	
Output Capacitance			pF typ	
LOGIC OUTPUT (F_{OUT})				
Output High Voltage, V_{INH}	2.4	2.4	V min	I Source = 800 µA except for $XCLK_{OUT}$
Output Low Voltage, V_{INL}	0.4	0.4	V max	I Sink = 1.6 mA except for $XCLK_{OUT}$
LOGIC INPUTS[3]				
ALL INPUTS EXCEPT $XCLK_{IN}$				
Input High Voltage, V_{INH}	2.0	2.0	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}	10	10	pF typ	
$XCLK_{IN}$ ONLY				
Input High Voltage, V_{INH}	3.5	3.5	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}	10	10	pF typ	
CLOCK FREQUENCY				
$XCLK_{IN}$	100	100	kHz min	For Specified performance
	5	5	MHz max	
POWER REQUIREMENTS				
V_{DD}	+5	+5	V nom	±5% for Specified Performance
I_{DD}	8	8	mA max	V_{DD} = 5V± 5%
Power Dissipation	40	40	mW max	Typically 30mW

NOTES

[1]Temperature Ranges are as follows: B Version, –40°C to +85°C; Y Version, –40°C to +125°C.

[2]See Terminology.

[3]Guaranteed by design and characterization, not production tested.

[4]The absolute input voltage on the different input pins must not go more positive than Vdd - 2V or more negative than GND - 400mV. The common-mode voltage applies to those inputs which form differential pairs.

Span = Max output frequency - Min output frequency

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2]

(V_{DD} = +5 V ± 5%, GND = 0 V, External Reference = +2.5 V; XCLK IN = 5MHz; All specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Limit at T_{MIN}, T_{MAX} (B Version)	Units	Conditions/Comments
F_{CLOCK}	100	kHz min	Clock Frequency
	5	MHz max	
t_{HIGH}/t_{LOW}	45/55	min	Clock Mark / Space Ratio
	55/45	max	
t_1	9	ns typ	CLK Edge to F_{OUT} Edge Delay
t_2	TBD	ns typ	F_{OUT} Rise Time
t_3	TBD	ns typ	F_{OUT} Fall Time

NOTES
[1]Sample tested at +25°C to ensure compliance.
[2]See Figure 1.
Specifications subject to change without notice

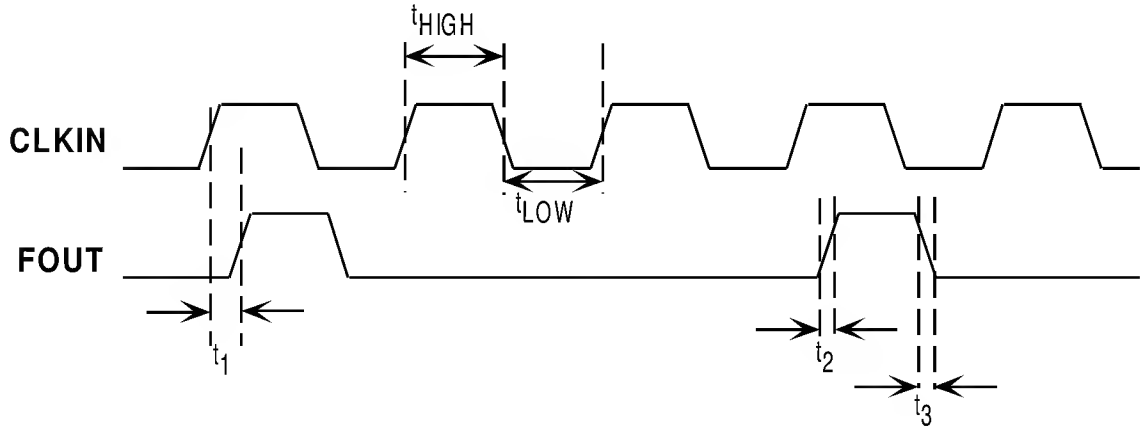


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to GND ..... –0.3 V to +7 V
Analog Input Voltage to GND ..... –5 V to +7V
Reference Input Voltage to GND .... –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND ..... –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
  Industrial (B Version) ..... –40°C to +85°C
  Automotive (Y Version) ..... –40°C to +125°C
  Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
Plastic DIP Package, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance (8-pin DIP) ..... 125°C/W
  θ_{JA} Thermal Impedance (16-pin DIP) ..... 117°C/W
  Lead Temperature (Soldering, 10 sec) ..... +260°C
SOIC Package, Power Dissipation ..... 450 mW
  θ_{JA} Thermal Impedance (8-Lead) ..... 157°C/W
  θ_{JA} Thermal Impedance (16-Lead) ..... 74°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) ..... +215°C
    Infrared (15 sec) ..... +220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

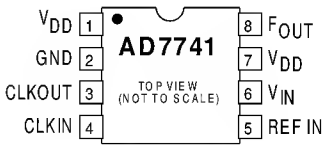
AD7741/42 ORDERING GUIDE

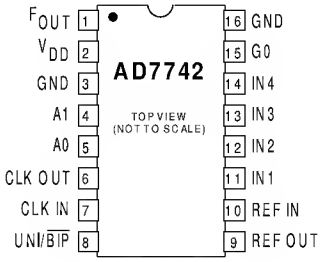
Model	Temperature Range	Package Option*
AD7741BN	-40°C to +85°C	N-8
AD7741BR	-40°C to +85°C	R-8
AD7741YR	-40°C to + 125°C	R-8
AD7742BN	-40°C to +85°C	N-16
AD7742BR	-40°C to +85°C	R-16A
AD7742YR	-40°C to + 125°C	R-16A

*N = Plastic DIP, R = SOIC.

PIN CONFIGURATION

DIP and SOIC





CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD7741 PIN FUNCTION DESCRIPTION

Pin No.	Pin Mnemonic	Description
1	V_{DD}	Positive supply voltage, +5 V ± 5%.
2	GND	Analog Ground. Ground reference for Programmable Gain Amplifier, Voltage to Frequency Con verter and Bandgap Reference.
3	CLKOUT	External Clock Output. When the master clock for the device is a crystal, the crystal is connected between CLKIN and CLKOUT. When an external clock is applied to CLKIN, CLKOUT pro-vides an inverted clock signal. This clock must be buffered before being used to provide a clock source for a microprocessor, ADC or other system components.
4	CLKIN	External Clock Input. The master clock for the device can be provided in the form of a crystal or an external clock. A crystal can be tied across the CLKIN, CLKOUT pins. Alternatively, the CLKIN pin can be driven with a CMOS-compatible clock and CLKOUT left unconnected.
5	REF IN	Voltage Reference Input. A precision reference (e.g. REF192) is applied to this pin.
6	V_{IN}	Analog Input Channel. The analog input range is from 0V to REF IN. An input signal equal to 0V results in an output frequency of F_{OUT} min (5% of F_{CLOCK}) and an input of REF IN results in an output frequency of F_{OUT} max (45% of F_{CLOCK}).
7	V_{DD}	Positive supply voltage, +5 V ± 5%.
8	FOUT	Frequency Output

AD7742 PIN FUNCTION DESCRIPTION

Pin No.	Pin Mnemonic	Description
1	FOUT	Frequency Output
2	V_{DD}	Positive supply voltage, +5 V ± 5%.
3	GND	Analog Ground.
4	A1	Channel Select Input. This is used as a channel select input in conjunction with A0 to select one of four possible input channel configurations allowable.
5	A0	Channel Select Input. This is used as a channel select input in conjunction with A1 to select one of four possible input channel configurations allowable.
6	CLKOUT	External Clock Output. When the master clock for the device is a crystal, the crystal is connected between CLKIN and CLKOUT. When an external clock is applied to CLKIN, CLKOUT provides an inverted clock signal. This clock must be buffered before being used to provide a clock source for a microprocessor, ADC or other system components.
7	CLKIN	External Clock Input. The master clock for the device can be provided in the form of a crystal or an external clock. A crystal can be tied across the CLKIN, CLKOUT pins. Alternately, the CLKIN pin can be driven with a CMOS-compatible clock and CLKOUT left unconnected.
8	UNI/$\overline{\text{BIP}}$	Unipolar/$\overline{\text{BIPOLAR}}$ Input Select. This pin determines whether the device is to operate with differential bipolar input signals (common mode range: -300mV to (V_{DD}-2V)) or whether the differential analog input signals are always positive. With UNI/$\overline{\text{BIP}}$ high, a differential analog input signal equal to 0 V results in an output frequency of F_{OUT} min (5% of F_{CLOCK}) and an input of REF IN/Gain results in an output frequency of F_{OUT} max (45% of F_{CLOCK}). With UNI/$\overline{\text{BIP}}$ low, a differential analog input signal of -REF IN/Gain results in an output frequency of F_{OUT} min (5% of F_{CLOCK}) and an input of +REF IN/Gain results in an output frequency of F_{OUT} max (45% of F_{CLOCK}).
9	REFOUT	Voltage Reference Output. A +2.5V reference is provided at this pin. REF OUT has a low output impedance which makes it suitable for directly driving external circuitry.
10	REFIN	Voltage Reference Input. This defines the span of the VFC. For specified operation a +2.5 V reference is required at this pin. It can be tied to REF OUT directly or, if a precision reference is available, it can be applied to this pin.
11	IN1	Analog Input Channel 1. This is either a pseudo-differential input with respect to IN4 or it is the positive input of a differential analog input pair when used with IN2 (See Table I). In bipolar made the differential analog input voltage range is ±REF IN /Gain of the PGA. In unipolar mode the differential analog input voltage range is 0 to +REF IN /Gain.
12	IN2	Analog Input Channel 2. This is either a pseudo-differential input with respect to IN4 or it is the negative input of a differential analog input pair when used with IN1 (See Table I).
13	IN3	Analog Input Channel 3. This is the positive input of a differential analog input pair when used with IN4 (See Table I).
14	IN4	Analog Input Channel 4. This is either the common input for pseudo-differential inputs on IN1 and IN2 or it is the negative input of a analog input pair when used with IN3 (See Table I).
15	G0	Gain Select Input. This is used as a gain select input for the PGA to select one of two gains for the PGA.
16	GND	Analog Ground. Ground reference for Programmable Gain Amplifier, Voltage to Frequency Converter and Bandgap Reference.

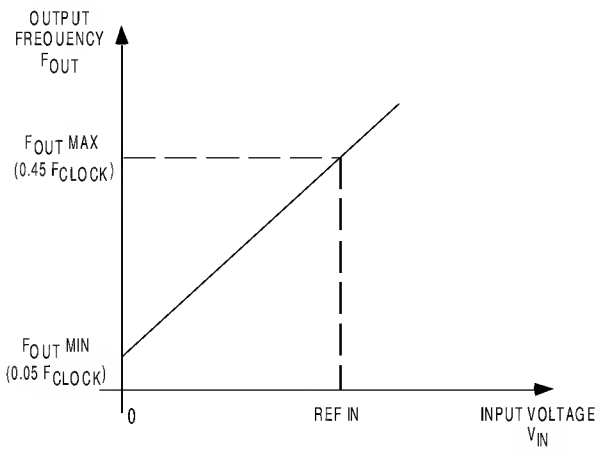


Figure 1. AD7741 Transfer Characteristic for Input Range from 0 V to REF IN.

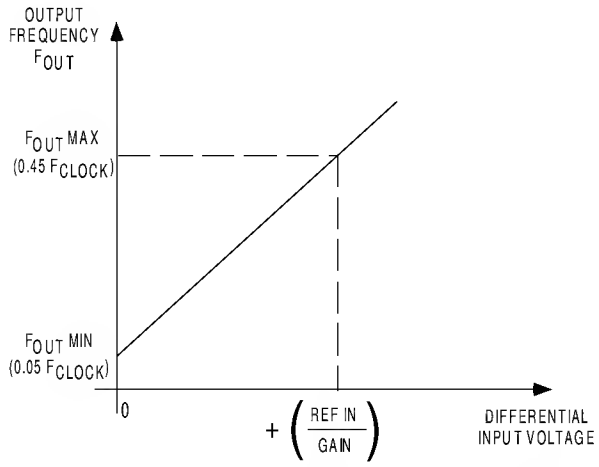


Figure 2. AD7742 Transfer Characteristic for Unipolar Differential input range: 0 V to REF IN/Gain; the input common mode Range must be between -300mV and V_{DD} -2V. UNI/$\overline{BIP}$ pin tied to V_{DD}.

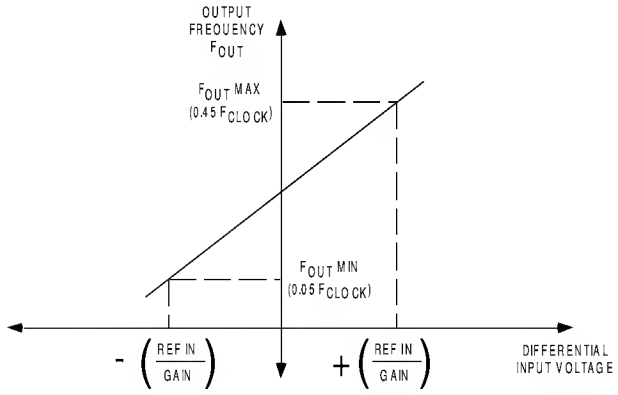


Figure 3. AD7742 Transfer Characteristic for Bipolar Differential Input Range: -REF IN/Gain to +REF IN/Gain (the common mode range is from -300mV to V_{DD} - 2 V). UNI/$\overline{BIP}$ pin tied to GND.

TABLE I. AD7742 INPUT CHANNEL SELECTION

A1	A0	IN(+)	IN(-)	TYPE
0	0	IN1	IN4	Pseudo Diff
0	1	IN2	IN4	Pseudo Diff
1	0	IN3	IN4	Full Diff
1	1	IN1	IN2	Full Diff

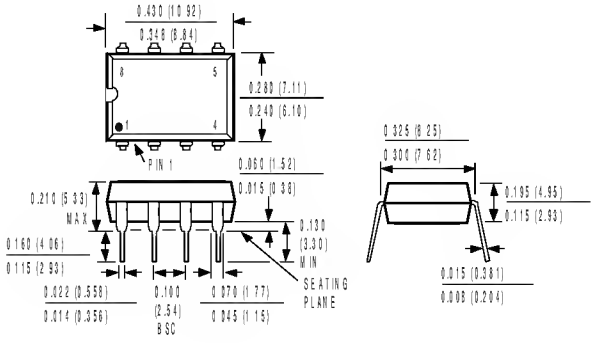
TABLE II. AD7742 GAIN SETTING SELECTION

UNI/BIP	G0	Gain Setting, G	Differential Input Voltage Span	
1	0	X1	0 to +2.5 V	0 to +REF IN/Gain
1	1	X2	0 to +1.25 V	0 to +REF IN/Gain
0	0	X1	-2.5 to +2.5 V	-REF IN/Gain to +REF IN/Gain
0	1	X2	-1.25 to +1.25 V	-REF IN/Gain to +REF IN/Gain

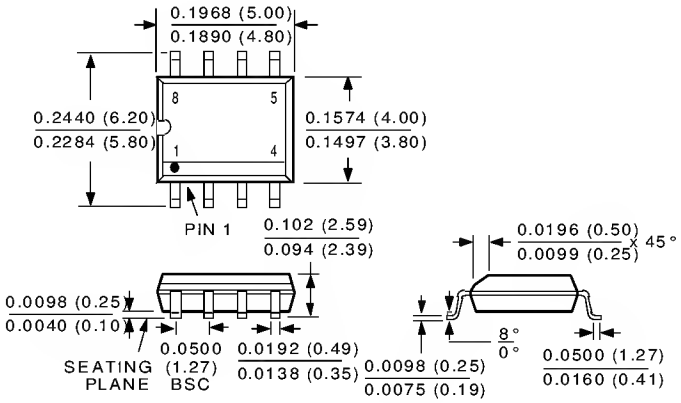
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

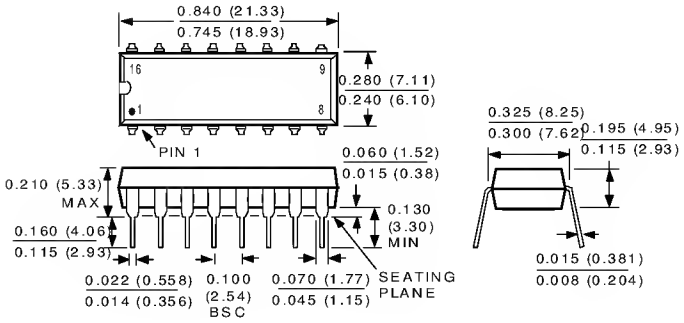
8-Pin Plastic DIP (N-8)



8-Lead SO (R-8)



16-Pin Plastic DIP (N-16)



16-Lead Narrow Body SO (R-16A)